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Title of the Invention

SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

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TITLE OF THE INVENTION
SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

5 The present invention relates to a semiconductor
integrated circuit device and, more particularly, to a
technique which is effective when applied, in a
semiconductor integrated circuit device including
circuits for processing signals from an intermediate-
10 frequency band to a high-frequency band, to a
protective technique for preventing the electrostatic
breakdowns of circuit elements constructing the
semiconductor integrated circuit device.

 A wireless communication system (or a wireless
15 communication mobile terminal device, as will be
shortly called the "terminal device") such as a
digital cellular system has its circuits of
transmission line and reception line constructed to
include many discrete ICs (semiconductor integrated
20 circuit devices). A representative example of the
terminal device, of which the transmission/reception
line circuits are constructed of the discrete ICs, is
shown in Fig. 9. The discrete ICs are serviced from
semiconductor parts makers such as NEC or RF Micro
25 Device.

On the other hand, the technique of integrating the transmission/reception units into one chip is described on pp. 17 to 20 of "Hitachi Review", Vol. 81, No. 10 (1999-10), issued by Hitachi Reviewer Co., Ltd.

On the other hand, the electrostatic breakdown protecting circuit of IC is disclosed in Japanese Patent Laid-Open No. 230266/1989, for example. In this Laid-Open, there is disclosed an electrostatic breakdown preventing circuit in which a plurality of diodes are connected in series between the terminal of an integrated circuit and a power supply line or a ground line.

In Japanese Patent Laid-Open No. 202583/1995, on the other hand, there is disclosed a CMOS protective circuit corresponding to the CMOS circuit in which a plurality of power supply voltages are mixed.

Here will be described the prior art with reference to the accompanying drawings. Fig. 9 is a schematic block diagram showing transmission/reception circuits or the like, which are packaged in the terminal device of the prior art. The ICs are individually made functionally discrete, and the portions, as individually enclosed by squares, are the discrete ICs.

In this block diagram, there are shown a transmission line and a reception line, which are connected with an antenna 1 through a duplexer 2. Both these transmission line and reception line are
5 connected with the not-shown base band.

The reception line is constructed by connecting the antenna 1, a band-pass filter 3 packaged in the duplexer 2, a low-noise amplifier 4, a band-pass filter 5, a reception mixer 6, a band-pass filter 7, a
10 variable-gain controlled amplifier 8 and a demodulator 9 sequentially in series. The demodulator 9 is connected with the not-shown base band.

The transmission line is constructed by connecting a modulator 11, a variable-gain controlled
15 amplifier 12, a transmission mixer 13, a band-pass filter 14, a transmission preamplifier 15, a high-output amplifier 16, a band-pass filter 17 packaged in the duplexer 2, and the antenna 1 sequentially in series. The modulator 11 is connected with the not-
20 shown base band. On the other hand, the demodulator 9 and the modulator 11 perform the frequency conversion in response to a station signal inputted from a VCO 18. The reception mixer 6 and the transmission mixer 13 also perform the frequency conversion in response
25 to the station signal from a VCO 19.

The signals (in electric waves) 10, as received by the antenna 1, are sequentially processed by the individual circuits of the reception line and are sent to the base band. On the other hand, the signals, as
5 sent from the base band, are sequentially processed by the individual circuits of the transmission line and are emitted as the electric waves 10 from the antenna 1.

The portions, as enclosed by the squares, are
10 the discrete ICs, as has been described hereinbefore. On the other hand, the internal small squares are electrostatic breakdown protecting circuits 20 (as will be called the "protective circuits").

In the construction of the prior art thus far
15 described, it is estimated from the handling notices described in the IC catalogue of each semiconductor parts maker that the variable-gain controlled amplifiers 8 and 12, the demodulator 9 and the modulator 11, or the intermediate-frequency band ICs
20 of several hundreds MHz are provided with the protective circuits 20 for preventing the circuit breakdowns, as might otherwise be caused by the electrostatic charges from several tens to several hundreds V, to enhance the high breakdown voltages.

25 On the other hand, the high-frequency band ICs

in the vicinity of 1 GHz such as the low-noise amplifier 4, the reception mixer 6, the transmission mixer 13, the transmission preamplifier 15 or the high-output amplifier 16 are described for the user to consider the static electricities, and it is also estimated that no protective circuit is included.

As one example of the protective circuit, there is known a protective circuit which is disclosed in Japanese Patent Laid-Open No. 202583/1995, as described hereinbefore. Fig. 10 is a schematic diagram in which a portion is added for easier illustration to the diagram of the protective circuit presented by the Laid-Open.

In Fig. 10, numeral 41 designates a protective circuit. Letter V designates an input or output signal to an integrated circuit, and this signal is inputted via a signal line 44 to an internal circuit 45 or outputted from the internal circuit 45. The protective circuit 41 is made of a diode-connected NMOS transistor 42 and an NMOS transistor 43. Specifically, the transistor 42 is connected at its shorted gate and drain with the signal line 44 and is connected at its source with a power supply voltage Vcc. On the other hand, the transistor 43 is connected at its drain with the signal line 44 and at

its shorted gate and source with the ground.

On the other hand, one example of the protective circuit having diodes connected at multiple stages is disclosed in Japanese Patent Laid-Open No.

5 230266/1989, as has been described hereinbefore.

Figs. 11 and 12 are schematic diagrams in which a portion is added to the diagrams of the diodes for forming the protective circuit and the electrostatic breakdown preventing circuit of that Laid-Open, so as
10 to facilitate the description.

As shown in Fig. 11, two diodes 51 and 52 are connected in series at two stages in the forward direction between the signal line 53 and the ground line 55 of an internal circuit 54. A signal is
15 transmitted via the signal line 53 to the internal circuit 54. Fig. 11 omits the protective circuit on the power supply side, the action of which is identical to that shown in Fig. 10.

By the two-stage construction, a Von voltage is
20 raised to suppress the electric current to flow through the protective circuit. Fig. 12 shows a sectional structure of the protective circuit elements constructed to have a two-stage connection. Over one face of a P-type substrate 61 forming an integrated
25 circuit, there is formed an N-type epitaxial layer 62.

On the surface side of this N-type epitaxial layer 62, there are formed a plurality of (or two, as shown) P-type diffusion layers 63 for wells. In the surface layer portion of the P-type diffusion layer 63, on the other hand, there is formed an N-type diffusion layer 64. Therefore, the P-type diffusion layer 63 and the N-type diffusion layer 64 form PN junction diodes (51 and 52).

Between the individual P-type diffusion layers 63, on the other hand, there is formed a P-type insulating diffusion layer 65 as a channel stopper. This P-type isolating diffusion layer 65 so extends all over in the thickness direction of the N-type epitaxial layer 62 as to reach the P-type substrate 61 at its lower end.

Over the surface on one side of the P-type substrate 61, on the other hand, there is formed a silicon dioxide film 66. This silicon dioxide film 66 is partially removed at its portion confronting the P-type diffusion layer 63 and the N-type diffusion layer 64, to form contact windows. Over the silicon dioxide film 66 including those contact windows, moreover, there is formed an aluminum deposited layer 67 in a predetermined pattern.

As a result, the two diodes 51 and 52 are

connected in series in the forward direction by the aluminum deposited layer 67, and one diode 51 is connected at its cathode electrode 68 with the signal line 53 of the internal circuit whereas the other
5 diode 52 is connected at its anode electrode 69 with the ground line 55.

SUMMARY OF THE INVENTION

In accordance with the miniaturization of the wireless communication mobile terminal device of
10 recent years, there has been desired and developed a one-chip IC in which the transmission/reception band modulator/demodulator circuits and the high-frequency amplifications are integrated to correspond to the
15 low-noise amplifier 4, the reception mixer 6, the variable-gain controlled amplifier 8, the demodulator 9, the modulator 11, the variable-gain controlled amplifier 12, the transmission mixer 13 and the transmission preamplifier 15, as shown in Fig. 9. It
20 is necessary to protect the entire chip against the high breakdown voltage.

However, it has been found out that the one-chip IC of the prior art incorporating the protective circuit has the following problems.

25 (1) The high-frequency circuit including the low-

noise amplifier 4, the reception mixer 6, the
transmission mixer 13 and the transmission
preamplifier 15 is provided at its input/output
circuits with a matching circuit having a capacity and
5 an inductance. With the inductance of this matching
circuit, for example, a high voltage is generated by
the change in the voltage at the input/output portions
of the integrated circuit. Moreover, the output
terminals of the individual circuits are biased in the
10 DC manner to the potential of the power supply
voltage. As a result, in response to the input
signal, a signal having a potential no less than the
power supply voltage is outputted. If the circuit
having a construction of transistors of one stage is
15 applied as the protective circuit as in the example of
the prior art, a bias condition for allowing the
electric current to flow through that protective
circuit is established to raise a problem that the
signal is distorted.

20 (2) On the other hand, the attachment of the
protective circuit of the prior art raises a problem
that the parasitic capacity is so high as to
deteriorate the gain. This makes it hard to apply the
protective circuit of the prior art to the circuit of
25 the high-frequency portion.

(3) In the protective circuit having the transistors of a construction of two stages of the prior art, on the other hand, the element structure is constructed of thyristors. If a high static electricity is applied, therefore, the IC actions cannot be made because an overcurrent continuously flows unless the power supply is broken.

The problems, as found out by our investigations to be caused by the protective circuit for the high-frequency circuit, will be described with reference to Figs. 13A and 13B and the subsequent Figures. First of all, the deterioration of the linearity will be described in the case of a circuit output.

Figs. 13A and 13B illustrate the static characteristics of the NMOS transistors 42 and 43 of Fig. 10 and the actions of the high-frequency signals. With the circuit construction shown in Fig. 10, in the action state in which the power supply of the IC and the ground are connected with the power supply line over the substrate, little electric current flows through the transistors of the protective circuit, but the desired signal voltage is applied to the internal circuit 45, when the signal voltage V_{cc} desired by the circuit is applied to the signal line 44.

Next, if a positive static electricity V_1 higher

than the voltage V_{on} , at which the transistors are turned ON, + the power supply voltage V_{cc} are applied to the signal line 44 at the time of handling the IC on the substrate, a diode forward current I flows
5 through the NMOS transistor 42, as shown in Fig. 13A, but no overcurrent flows through the internal circuit so that the internal circuit 45 is protected.

Likewise for a high negative static electricity, if an electrostatic voltage V_2' no higher than $-V_{on}$
10 is applied, as shown in Fig. 13B, a diode forward current I' flows through the transistor 43 to protect the internal circuit 45.

Here, the high-frequency circuit adopts the method the matching is made by connecting the source
15 terminal directly with the outside of the IC and by using the capacity and the inductance so as to amplify the output drastically, the power supply voltage is applied to the IC output terminal.

The internal circuit 45 of Fig. 10 corresponds
20 to the low-noise amplifier 4, the reception mixer 6, the transmission mixer 13 or the transmission preamplifier 15 of Fig. 9, for example. When the power supply voltage V_{cc} is applied to the signal line 44 to superpose a high-frequency signal, a high-
25 frequency voltage 46 around the graph origin of Fig.

13A is applied to the transistor 42. If the high-frequency voltage amplitude is no more than V_{on} , little high-frequency current flows through the transistor 42, and the current amplitude of the internal circuit is outputted. If the voltage amplitude becomes large over V_{on} , however, a nonlinear high-frequency current 47 flows to the transistor 42 so that it is superposed on the output current amplitude of the internal circuit to distort the output signal.

Under this action condition, the input amplitude of the desired wave of the reception circuit is at V_{on} or smaller so that the distortion raises no serious problem. If the interfering wave in the near band, as cannot be filtered out by the upstream circuit stage, is so large as to have a voltage amplitude at V_{on} or higher, however, the interfering wave causes a distortion to deteriorate the S/N characteristics in the reception band. In the transmission circuit, on the other hand, the desired wave has a large output amplitude so that the S/N deterioration occurs likewise at the distortion by the desired wave.

Here will be described the case of the input point of the circuit. Where the circuit includes enhancement type transistors such as Si bipolar

transistors having a bias voltage at about +1 V at their input points, the protective circuit is normally OFF even if the high-frequency voltage amplitude is inputted, so that no electric current flows through
5 the protective transistors thereby not to distort the input signal. In the case of the depression type such as the GaAs FETs, however, when a negative voltage $V_{3'}$ is applied to the signal line so that the high-frequency signal is superposed, as shown in Fig. 13B,
10 a high-frequency voltage 48 around $V_{3'}$ is applied to the transistor 43. If the high-frequency voltage is no higher than $-V_{on}$, it hardly flows through the transistor 43 so that the signal is transmitted as it is to the internal circuit.

15 If the voltage exceeds the value of $-V_{on}$ to a large amplitude, however, a nonlinear high-frequency current 49 flows through the transistor 43 and is superposed over the input current amplitude of the internal circuit to distort the input signal.

20 If the input signal has a distortion, this distortion is amplified by the internal circuit so that the amplified distortion is superposed on the distortion to be caused in the intrinsic signal, thereby to deteriorate the linearity. Like the
25 aforementioned time of the output signal, the S/N

ratio is deteriorated. This is because the protective circuit for the transistors of one stage diode-connected are provided on the power supply side and on the ground side for the signal lines.

5 In order to solve this problem, there is a method in which the diode-connected transistors are connected in series to raise the voltage V_{on} so that little electric current may flow at the desired voltage for the internal circuit to act, as in the
10 aforementioned protective circuit having the two-stage construction of Fig. 11. Moreover, the series connection reduces the parasitic capacity and the deterioration in the frequency characteristics.

 According to this structure, however, a portion,
15 as designated by 70 in Fig. 12, is given the thyristor structure by inserting the P-type diffusion layer of the channel stopper. The action principle of the thyristor is shown in Fig. 14. The thyristor is in the turn-OFF state to allow little electric current to
20 flow, when it is in the forward voltage state and at a low voltage. When the voltage rises high, the thyristor is turned ON to allow a large electric current to flow. Therefore, the protective circuit of the diode construction having the multistage
25 connection may be turned ON with a high voltage of

static electricity. In order to prevent this, the power supply has to be broken. This breakdown is difficult to realize for the transistor structure of the prior art.

5 In the construction where the electric current flows from the ground to the power supply, as shown in Fig. 10, no problem arises, when the power supply and the ground of the IC are connected with the wiring lines of the substrate so that the power is supplied.

10 When the IC is charged while being handled for its assembling work, however, the protective circuit may not function. With the IC being in the floating state and with the ground being open, for example, if a plus (+) or minus (-) potential difference is established

15 between the voltage V_{cc} and the signal line 44, the voltage V_{cc} on the plus side with respect to the minus side of the signal line becomes inverse so that no electric current flows through the protective circuit. In other words, the protective circuit is weak against

20 the negative static electricity with respect to the voltage V_{cc} , and the internal circuit may be broken by the high negative static electricity.

 An object of the invention is to provide a semiconductor integrated circuit device for wireless

25 communications, which has an electrostatic breakdown

protecting circuit capable of protecting an IC
reliably against positive/negative static
electricities.

Another object of the invention is to provide a
5 semiconductor integrated circuit device for wireless
communication, which has a protective circuit capable
of protecting a low-frequency circuit (including a
circuit of an intermediate-frequency band) and a
circuit of a high-frequency band against the
10 electrostatic breakdown.

Still another object of the invention is to
provide a semiconductor integrated circuit device for
wireless communications, which is excellent against
the electrostatic breakdown while preventing the
15 deteriorations of the linearity and gain of the high-
frequency circuit.

The aforementioned and other objects and novel
features of the invention will become apparent from
the following description to be made with reference to
20 the accompanying drawings.

A representative of the invention to be
disclosed herein will be briefly described in the
following.

For the circuit (or the low-frequency circuit)
25 of the intermediate-frequency, protective circuits

including diode-connected transistors of one stage are individually disposed on power supply lines and the ground line. For the circuit of the high-frequency band of the IC, there are incorporated, as the
5 protective circuit having a low parasitic capacity and little deterioration of signal characteristics, multistage protective circuits in which the voltage V_{on} is not exceeded even when a signal at the power supply voltage or higher is applied, in accordance
10 with the action point of the applied circuit, and multistage protective circuits which are not turned ON even when a signal exceeding a negative bias potential is applied. On the other hand, the protective circuits are constructed to protect the IC,
15 irrespective of the polarity of the static electricities to be established while the IC is being handled. Specifically, the protective circuits include: a first protective circuit for allowing an electric current to flow from a power supply line to
20 signal lines at a protection time against an electrostatic breakdown; a second protective circuit for allowing an electric current to flow from the signal lines to the ground line; a third protective circuit for allowing an electric current to flow from
25 the signal lines to the power supply line; and a

fourth protective circuit for allowing an electric current to flow from the ground line to the signal lines. Moreover, the diode-connected transistors of the multistage connection are given a structure in which the elements (i.e., the diode-connected transistors) are isolated by an insulator capable of the thyristor action.

According to the means thus far described, (a) in the semiconductor integrated circuit device, each internal circuit of the high-frequency band is provided at its input/output portions with the protective circuit of the multistage structure so that the internal circuit can be prevented from the electrostatic breakdown, as might otherwise be caused by the high positive/negative static electricities. On the other hand, each internal circuit of the low-frequency band is provided at its input/output portions with the protective circuit of one stage so that it can be prevented from the electrostatic breakdown, as might otherwise been caused by the positive/negative static electricities.

(b) The output terminal of each internal circuit of the high-frequency band is biased to the power supply voltage so that a signal at an output voltage or higher is outputted in response to the

input signal. Where the protective circuit is made of the circuit including transistors of one stage construction, as in the prior art, therefore, the bias condition for the electric current to flow through the protective circuit is raised to distort the signal.

In the invention, on the contrary, this signal distortion can be suppressed because the protective circuit of the multistage structure is adopted.

(c) The transistors are formed in the semiconductor regions which are electrically insulated from one another, so that the formation of the thyristor, as might otherwise be formed by the two-stage construction of transistors of the prior art, can be prevented.

(d) The protective circuit, as disposed at the input/output portions of each internal circuit of the high-frequency band is constructed to include the diode-connected transistors of the multistage structure. Therefore, the parasitic capacity is lowered to reduce the deterioration of the linearity or the gain of the high-frequency circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram showing a protective circuit to be incorporated into an internal circuit in

a semiconductor integrated circuit device according to one embodiment (Embodiment 1) of the invention;

Figs. 2A and 2B are diagrams showing individual current paths at the times when the protective circuit
5 protects electrostatic breakdowns caused by positive/negative static electricities;

Fig. 3 is a circuit diagram showing a circuit in which the protective circuit is incorporated into an amplifier circuit as an internal circuit;

10 Fig. 4 is a characteristic diagram of the amplifier circuit;

Fig. 5 is a block diagram showing a construction of a wireless communication system having the semiconductor integrated circuit device of Embodiment
15 incorporated thereinto;

Fig. 6 is a sectional diagram showing diode-connected transistors constructing a protective circuit in the semiconductor integrated circuit device;

20 Fig. 7 is a circuit diagram showing a protective circuit to be incorporated into a low-frequency internal circuit of the wireless communication system;

Fig. 8 is a circuit diagram showing a protective circuit to be incorporated into an internal circuit of
25 a semiconductor integrated circuit device according to

another embodiment (Embodiment 2) of the invention;

Fig. 9 is a block diagram showing a construction of a wireless communication system having the semiconductor integrated circuit device incorporated thereinto;

Fig. 10 is a circuit diagram showing a protective circuit;

Fig. 11 is a circuit diagram showing another protective circuit;

Fig. 12 is a schematic sectional diagram showing a transistor construction to be used in a protective circuit;

Figs. 13A and 13B are characteristic diagrams illustrating the static characteristics used in a protective circuit of transistors and the actions of a high-frequency signal; and

Fig. 14 is a schematic diagram showing a structure and an action principle of a thyristor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The invention will be described in detail in connection with its embodiments with reference to the accompanying drawings. Here, throughout all the Figures for explaining the embodiments of the invention, the parts having the same functions are

designated by the same reference numerals, and their repeated description will be omitted.

[Embodiment 1]

5 Figs. 1 to 7 are diagrams relating to a semiconductor integrated circuit device according to one embodiment (Embodiment 1) of the invention, and Figs. 1 to 5 are diagrams relating to a protective circuit.

10 In Embodiment 1, the invention will be described on the example in which it is applied to a signal processing IC for a cellular phone. Here will be described a construction of the cellular phone. Fig. 5 is a block diagram showing a portion of a system construction of the cellular phone.

15 In this block diagram, as in Fig. 9, there are shown a transmission line and a reception line which are connected with an antenna 1 through a duplexer 2. Both of these transmission line and reception line are connected with a not-shown base band.

20 The reception line is constructed by connecting the antenna 1, a band-pass filter 3 packaged in the duplexer 2, a low-noise amplifier 4, a band-pass filter 5, a receiving mixer 6, a band-pass filter 7, a variable-gain controlled amplifier 8 and a demodulator
25 9 sequentially in series. The demodulator 9 is

connected with the not-shown base band.

The transmission line is constructed by connecting a modulator 11, a variable-gain controlled amplifier 12, a transmission mixer 13, a band-pass filter 14, a transmission preamplifier 15, a high-output amplifier 16, a band-pass filter 17 packaged in the duplexer 2, and the antenna 1 sequentially in series. The modulator 11 is connected with the not-shown base band. On the other hand, the demodulator 9 and the modulator 11 performs frequency conversions in response to a local oscillation signal inputted from a VCO 18. The reception mixer 6 and the transmission mixer 13 also perform frequency conversions in response to a local oscillation signal inputted from a VCO 19.

A signal (in electric waves), as received by the antenna 1, is sequentially processed by the individual circuit of the reception line and is set to the base band. On the other hand, a signal sent from the base band is sequentially processed by the individual circuits of the transmission line and is emitted as the electric waves 10 from the antenna 1. The signal 10, as emitted from the antenna 1, and the signal 10, as received by the antenna 1, are exemplified to have a high-frequency band of 1 GHz, but signals of a low-

frequency band are processed by the demodulator 9, the modulator 11 and so on for transferring signals with the base band. The signals of the low-frequency band are exemplified to have an intermediate-frequency band-
5 of several hundreds MHz.

In Embodiment 1, the individual circuit elements (of internal circuits) for processing signals, as including the low-noise amplifier 4 are monolithically packaged in a single semiconductor IC chip 25, as
10 enclosed by solid lines in Fig. 5. In this semiconductor IC chip 25, more specifically, there are monolithically packaged as the internal circuits the low-noise amplifier 4, the reception mixer 6, the variable-gain controlled amplifier 8, the demodulator
15 9, the VCO (Voltage Controlled Oscillator) 18, the modulator 11, the variable-gain controlled amplifier 12, the transmission mixer 13, the transmission preamplifier 15 and the VCO 19.

At the input/output portions of the
20 semiconductor IC chip 25, respectively, there are provided protective circuits which are made to stand high voltages for preventing the electrostatic breakdowns, as might otherwise be caused by the electrostatic charges (or positive/negative static
25 electricities) from several tens to several hundreds

V, of the internal circuits. These protective circuits are exemplified by protective circuits 26 of a multistage structure, in which a plurality of diode-connected transistors are connected in series, for a high-frequency band, and protective circuits 27 of one stage, in which one diode-connected transistor is used, for a low-frequency band or an intermediate-frequency band.

The protective circuit 26 of the multistage structure is disposed at the input/output portion of each of the low-noise amplifier 4, the reception mixer 6 and the transmission preamplifier 15, at the input portion of the variable-gain controlled amplifier 8, and at the output portion of the transmission mixer 13. The protective circuit 27 of the one stage is disposed at the output portion of the demodulator 9 and at the input portion of the modulator 11.

Here will be described the protective circuit 26 of the multistage structure to be disposed at the input/output portions of the high-frequency band, with reference to Figs. 1 to 4.

The protective circuit 26 of the multistage structure is constructed, as shown in Fig. 1 and Figs. 2A and 2B, by arranging a diode of the multistage structure between a signal line 30, and a power supply

line 31 and a ground line 32, as connected with an internal circuit 29. Letter V appearing in Fig. 1 designates an input signal or an output signal to or from the internal circuit 29 so that it is inputted or
5 outputted via the signal line 30 to or from the internal circuit 29.

The protective circuit 26 of the multistage structure is constructed, as shown in Figs. 2A and 2B, of: a first protective circuit A in which an electric
10 current flows via route (1) from the power supply line 31 to the signal line 30 at the electrostatic breakdown protecting time; a second protective circuit B in which an electric current flows via route (2) from the signal line 30 to the ground line 32; a third
15 protective circuit C in which an electric current flows via route (3) from the signal line 30 to the power supply line 31; and a fourth protective circuit D in which an electric current flows via route (4) from the ground line 32 to the signal line 30. The
20 first protective circuit A and the second protective circuit B prevent the electrostatic breakdown of the internal circuit 29 due to the negative static electricity, and the third protective circuit C and the fourth protective circuit D prevent the
25 electrostatic breakdown of the internal circuit 29 due

to the positive static electricity.

The diodes constructing the protective circuits are exemplified by diode-connected bipolar transistors and are kept from causing the thyristor phenomenon by
5 the later-described structure.

The third protective circuit C is given a multistage structure in which a plurality of bipolar transistors 1211 to 121n all diode-connected by shorting their bases and emitters are connected in
10 series. The transistor 1211 at the first stage is connected at its collector with a power supply Vcc (or the power supply line 31) and at its emitter with the collector of the transistor at the downstream stage. The transistor 121n at the n-th stage is connected at
15 its collector with the emitter of the transistor at the upstream stage and at its emitter with the signal line 30. Each transistor at the (n-1)-th stage from the second stage is connected at its collector with the emitter of the transistor at the upstream stage
20 and at its emitter with the collector of the transistor at the downstream stage.

The fourth protective circuit D is given a multistage structure in which a plurality of bipolar transistors 1221 to 122m all diode-connected by
25 shorting their bases and emitters are connected in

series. The transistor 1221 at the first stage is connected at its collector with a signal line 30 and at its emitter with the collector of the transistor at the downstream stage. The transistor 122m at the m-th-
5 stage is connected at its collector with the emitter of the transistor at the upstream stage and at its emitter with the ground (or the ground line 32). Each transistor at the (m-1)-th stage from the second stage is connected at its collector with the emitter of the
10 transistor at the upstream stage and at its emitter with the collector of the transistor at the downstream stage.

By thus raising the Von of the transistors 1211 to 121n connected with the power supply, the
15 transistors are turned OFF at a desired active voltage of the internal circuit 29 so that no electric current may flow. By likewise lowering the -Von of the transistors 1221 to 122m connected with the ground, the transistors are turned OFF at a desired active
20 voltage of the internal circuit 29 so that no electric current may flow.

The first protective circuit A is connected in parallel with the third protective circuit C and is formed of a breakdown protective circuit and diodes of
25 a multistage connection structure. Specifically, the

first protective circuit A is constructed to include:
a MOS transistor 1231 constructing the breakdown
protective circuit between the power supply Vcc (or
the power supply line 31) and the signal line 30; and
5 a plurality of bipolar transistors 1241 to 124i
connected between the MOS transistor 1231 and the
signal line 30. These transistors 1241 to 124i having
a structure, in which bases and emitters are all
diode-connected, and are connected in series with one
10 another to make the multistage structure as a whole.

The MOS transistor 1231 is connected at its
drain (or its one electrode) connected with the power
supply line 31, at its source (or its other electrode)
with the emitter of the first-stage transistor 1241,
15 and at its gate with the ground line 32. The
collector of the transistor 1241 at the first stage is
connected with the emitter of the transistor at the
downstream stage. The transistor 124i at the i-th
stage is connected at its emitter with the collector
20 of the transistor at the (i-1)-th stage and at its
collector with the signal line 30. Each transistor at
the (i-1)-th stage from the second stage is connected
at its emitter with the collector of the transistor at
the upstream stage and at its collector with the
25 emitter of the transistor at the downstream stage.

The second protective circuit B is connected in parallel with the fourth protective circuit D and is formed of a breakdown protective circuit and diodes of a multistage connection construction. Specifically, 5 the second protective circuit B is constructed to include: a plurality of bipolar transistors 125l to 125k having bases and emitters diode-connected between the signal line 30 and the ground line 32 (or the ground) and connected in multiple stages in series; 10 and a MOS transistor 1261 connected between the collector of the transistor 125k and the ground line 32 to construct the breakdown protective circuit. The MOS transistor 1261 is connected at its drain (or its one electrode) with the collector of the transistor 15 125k and connected at its gate and source (or its other electrode) with the ground line 32.

In the protective circuit 26 thus constructed, when the semiconductor IC chip 25 is handled, the paths of the electrostatic currents at the individual 20 potential differences in the power supply line, the ground line and the signal line are shown in Figs. 2A and 2B. For conveniences of the description, the first protective circuit A and the second protective circuit B are constructed to include transistors of 25 one stage, and the third protective circuit C and the

fourth protective circuit D are constructed to include transistors of two stages. These individual transistors are simply shown as diodes.

Fig. 2B shows the potential relations among the power supply (Vcc), the ground (GND) and the signal line (S), and which of the current paths (1) to (4) the electric current flows through in the circuits. The MOS transistor allows the electric current to flow by the punch through or the source-follower when a high static electricity is applied. As apparent from Fig. 2B, a current path is at any potential difference at any portion so that no overcurrent flows through the internal circuit 29.

If it is considered that a desired positive voltage is applied to the internal circuit 29, on the other hand, the transistors 1221 to 122m and transistors 1241 to 124i are reversely biased to cause no unnecessary leakage current to the power supply. The transistors 1211 to 121n are not turned ON either at a voltage of $(V_{cc} + V_{on} \times n)$ or lower. Nor is caused the punch-through by the transistor 1261 at the desired voltage so that no leakage occurs to the ground.

Where the desired voltage is negative, the transistors 1251 to 125k and the transistors 1211 to

121n are reversely biased. The transistors 1221 to 122m are not turned ON either up to $-V_{on} \times m$. Nor flows the electric current through the MOS transistor 1231. Therefore, the signal is correctly transmitted
5 between the internal circuit 29 and the terminal (V).

These bipolar transistor is given a structure, as shown in Fig. 6. The bipolar transistor is formed over an SOI (Silicon On Insulator) substrate 71 which is prepared by laminating an insulator such as a
10 silicon dioxide layer 73 over a silicon substrate 72. Over the SOI substrate 71, there is formed an N-type epitaxial layer 74. In this N-type epitaxial layer 74, there are selectively formed endless grooves by the dry-etching method or the like. These groove
15 extend so far as to reach the silicon dioxide layer 73. Moreover, the grooves are filled with an insulator 75. For example, the grooves are filled with silicon dioxide by the CVD (Chemical Vapor Deposition) method. Therefore, the N-type epitaxial
20 layer 74, as enclosed by the insulator 75, is an electrically independent region. In this region, there is formed the transistor.

In the surface layer portion of the N-type epitaxial layer 74 enclosed by the insulator 75, there
25 is formed a P-type diffusion layer 76. This region is

employed as the base region. In the surface layer portions of the P-type diffusion layer 76 and the N-type epitaxial layer 74, there are formed N-type diffusion layers 77 and 83. The region 77 is employed
5 as the collector region. The N-type diffusion layer 83, as formed in the surface layer portion of the P-type diffusion layer 76, is the emitter region.

Over the N-type epitaxial layer 74, the insulator 75, the P-type diffusion layer 76 and the N-
10 type diffusion layers 77 and 83, on the other hand, there is formed a silicon dioxide layer 78. This silicon dioxide layer 78 is partially removed at the portions confronting the emitter/base/collector regions to form contact holes. In the regions
15 including these contact holes, moreover, wiring lines are formed in a predetermined pattern. These wiring lines form a collector electrode 80, a base electrode 81 and an emitter electrode 82.

Thus, the silicon dioxide layer 73 and the
20 insulator 75 are used as barriers to form transistors which are so electrically isolated from one another as to form no thyristor. In Fig. 6, the emitter electrode 82 and the base electrode 81 are connected by a wiring line 79 to make a diode construction, and
25 these constructions are connected at multiple stages .

in series to construct the protective circuit.
Although the bipolar transistors have been exemplified
in the description thus far made, a similar
electrically insulating structure (or an isolation
5 structure) is also used when a MOSFET is constructed.
The structure of this transistor is applied to the MOS
transistor 1231 in the IC circuit. Fig. 7 is a
circuit diagram showing the aforementioned protective
circuit 27 of one stage. In Fig. 7, the protective
10 circuit A is constructed of the MOS transistor 1231
forming the breakdown protective circuit. This MOS
transistor 1231 is connected at its drain with the
power supply line 31, at its source with the signal
line 30 and at its gate with the ground line 32. This
15 breakdown protective circuit can be deemed as a
protective circuit of a source-follower transistor.

The second protective circuit B, as shown in
Fig. 7, has the MOS transistor 1261 constructing the
breakdown protective circuit, and this MOS transistor
20 1261 is connected at its drain with the signal line 30
and at its source with the ground line 32. This
breakdown protective circuit can be deemed as a
protective circuit of the surface breakdown.

The third protective circuit C is constructed of
25 the bipolar transistor 1211. This transistor 1211 is

connected at its collector with the power supply line 31 and at its emitter with the signal line 30.

The fourth protective circuit D is constructed of the bipolar transistor 1221. This transistor 1221
5 is connected at its collector with the signal line 30 and at its emitter with the ground line 32.

This protective circuit 27 of the one stage prevents the damage of the internal circuit 29 due to the positive/negative static electricities like the
10 aforementioned protective circuit 26 of the multistage structure.

Here will be described a more specific example of the circuit construction of the invention. This embodiment is especially effective when the integral
15 circuit is constructed of a BiCMOS (BiP transistor, a P-type MOS transistor or an N-type MOS transistor).

Fig. 3 shows one example of the case in which a high-frequency amplifier corresponding to the low-noise amplifier 4 of Fig. 5 is applied as the internal
20 circuit and in which the protective circuit of the invention is disposed at the output stage. A portion 90, as enclosed by a frame, is a circuit in the IC containing the protective circuit. Circuits 95 and 96 outside of the IC are input and output matching
25 circuits, respectively. The amplifier is a current-

mirror type amplifier which is fed with a voltage V_b to feed a constant current to a transistor 93 and which is fed with a high-frequency input voltage V_{in} to output a signal at an amplified voltage V_{out} . In the circuit diagram, a portion 91 is a protective circuit which is constructed to include transistors 92a to 92i having the structure shown in Fig. 6 and isolated electrically from one another. The internal transistor 93 is fed at its collector 94 with the same voltage of 3 V as the power supply voltage via the inductor of the output matching circuit 96. If the protective circuit has only the transistor 92a of one stage, there appears at the collector terminal 94 a superposition of a forward current, which flows from the protective circuit to the power supply voltage of 3 V in accordance with the characteristics of the exponential function of the bipolar transistor, and an amplifier output current which is generated by the transistor 93. The voltage amplitude of the amplifier raises no problem, when it is extremely small, but the nonlinear current to flow through the transistor of the protective circuit increases to cause a distortion as the amplitude becomes large. In order that the voltage V_{on} at which the transistor in the protective circuit begins to become conductive may be at 4 V as

the voltage capable satisfying the dynamic range of
the amplifier, the transistors of the protective
circuit are connected at three stages in series to
establish no electric flow at the circuit action
5 point. The circuit of the example needs no negative
power supply. By making the transistor of one stage
to be connected with the ground, therefore, the
circuit is protected even if a low negative static
electricity is applied. By this protective circuit,
10 moreover, the IC is protected, as described above,
even the static electricity is established at the time
of handling the IC.

Fig. 4 plots the input/output characteristics of
the amplifiers when the transistors to be connected
15 with the power supply in the protective circuit are
stacked at one stage and at three stages. As apparent
from Fig. 4, the one-stage series connection is
changed to the three-stage series connection, the
compression point of 1 dB is changed from -15 dBm to -
20 8 dBm so that the linearity is improved. Since the
collector-emitter capacity of the individual
transistors are connected in series, moreover, the
parasitic capacity of the protective circuit is
reduced, as compared with that of the protective
25 circuit of the prior art which is constructed to

include transistors of one stage diode-connected individually with the power supply and the ground, so that the gain of the amplifier is less deteriorated. The circuit for the intermediate-frequency band has
5 such a low frequency that the characteristic deterioration due to the parasitic capacity is remarkably small even in the protective circuit of the prior art. On the other hand, the adjoining transistors are isolated by the insulator or the
10 silicon dioxide layer so that they do not act as the thyristor.

The description thus far made is exemplified by the output point of the enhancement type transistor. In the case of the depression type transistor input as
15 in a GaAs FET, however, a nonlinear current is superposed on the input signal and is amplified to deteriorate the linearity likewise, if the voltage of $-V_{on}$ of the transistor to be connected with the ground is higher than the voltage to be applied to the gate
20 of the transistor. This makes it necessary to provide such a protective circuit on the input side, too, that the transistors to be connected with the ground are connected in series to lower the voltage of $-V_{on}$. Thus, the number of series of the transistors is
25 determined by the action point of the internal circuit

and by the target value of the compression point of 1 dB.

The semiconductor integrated circuit device of Embodiment 1 has the following effects.

5 (1) In the semiconductor integrated circuit device, each internal circuit 29 of the high-frequency band is provided at its input/output portions with the protective circuit 26 of the multistage structure so that the internal circuit 29 can be prevented from the
10 electrostatic breakdown, as might otherwise be caused by the high positive/negative static electricities. On the other hand, each internal circuit of the low-frequency band is provided at its input/output portions with the protective circuit 27 of one stage
15 so that it can be prevented from the electrostatic breakdown, as might otherwise been caused by the positive/negative static electricities.

Here, if the protective circuits of the high-frequency circuit portion are connected in series, as
20 described hereinbefore, the voltage V_{on} rises so that the current hardly flows to lower the electrostatic breakdown, as compared with the protective circuits of the intermediate-frequency band. However, the electrostatic voltage to break the IC (or the internal
25 circuit) is at a level of several tens to several

hundreds V, which is far higher than that of the IC to act at such a low power supply voltage as the invention is applied to. Therefore, a slight reduction in the breakdown voltage, as caused by
5 raising the voltage V_{on} , raise no problem.

(2) The output terminal of each internal circuit 29 of the high-frequency band is biased to the power supply voltage of a DC value so that an output voltage according to the input signal is produced at the
10 output terminal. This output voltage is changed around the bias voltage (at about the power supply voltage) by the inductance connected with the output terminal. Where the protective circuit is made of the circuit including transistors of one stage
15 construction, as in the prior art, therefore, the bias condition for the electric current to flow through the protective circuit is raised to distort the signal. In the invention, on the contrary, this signal distortion can be suppressed because the protective
20 circuit of the multistage structure is adopted.

(3) The transistors are formed in the semiconductor regions which are electrically insulated from one another, so that the formation of the thyristor, as might otherwise be formed by the two-stage
25 construction of transistors of the prior art, can be

prevented.

(4) The protective circuit, as disposed at the input/output portions of each internal circuit 29 of the high-frequency band is constructed to include the
5 diode-connected transistors of the multistage structure. Therefore, the parasitic capacity is lowered to deteriorate neither the linearity nor the gain of the high-frequency circuit.

(5) The two kinds of protective circuits, i.e., the
10 protective circuit 26 of the multistage structure and the protective circuit 27 of the one stage are disposed in the one-chip IC so that a high breakdown voltage can be established against the electrostatic breakdown of the entirety.

15 [Embodiment 2]

Fig. 8 shows a protective circuit of a semiconductor integrated circuit device according to another embodiment (Embodiment 2) of the invention. In the aforementioned protective circuit of the
20 multistage structure of Embodiment 1 shown in Fig. 1, the bipolar transistors are replaced as the diode-connected transistors by MOSFETs in accordance with Embodiment 2. These MOSFETs are diode-connected by shorting their gates and sources.

25 The first protective circuit A is constructed to

include: a MOSFET (transistor) 4331 connected between the power supply line 31 and the signal line 30 for forming a breakdown protective circuit; and a plurality of MOSFETs 4341 to 434i connected between
5 the MOSFET (transistor) 4331 and the signal line 30. The second protective circuit B is constructed to include: a plurality of MOSFETs (transistors) 4351 to 435k connected in series at multiple stages between the signal line 30 and the ground line 32; and a
10 MOSFET (transistor) 4361 connected with the MOSFET 435k for forming a breakdown protective circuit. The third protective circuit C is constructed to include a plurality of MOSFETs (transistors) 4311 to 431n connected in series. The fourth protective circuit D
15 is constructed to include a plurality of MOSFETs (transistors) 4321 to 432m connected in series.

In the protective circuit 26 of the multistage structure thus constructed, too, the electrostatic breakdown of the internal circuit 29, as might
20 otherwise be caused by the positive/negative static electricities, can be prevented as in Embodiment 1.

Although our invention has been specifically described on the basis of its embodiments, it should not be limited thereto but could naturally be modified
25 in various manners without departing from the gist

thereof.

The description thus far made is directed mainly to the case in which our invention is applied to the semiconductor integrated circuit device to be
5 incorporated into the wireless communication system belonging to the application field backgrounding the invention, but the invention should not be limited thereto. The invention can be applied to the semiconductor integrated circuit device for processing
10 the signals.

The effects to be obtained by the representative of the invention disclosed herein will be briefly described in the following.

(1) In the one-chip IC integrating the high-
15 frequency band and the intermediate-frequency band, according to the invention, the high-frequency circuit is provided with the protective circuits connected at multiple stages and in series, in addition to the protective circuit which is applied to the
20 intermediate-frequency band and which is constructed to include diode-connected transistors of one stage of the prior art, so that the parasitic capacity can be lowered while raising the voltage V_{on} to prevent the deterioration of the gain or the linearity.

25 (2) By thus providing the IC chip with two kinds of

protective circuits of different structures as the individual circuits therein, on the other hand, the total area of the protective circuits in the chip can be made smaller than that of the structure in which
5 the protective circuits of the multistage connection are applied to all the circuits in the IC.

(3) Thus, it is possible to realize the high breakdown voltage of the entire IC against the static electricity.

10 (4) It is possible to provide a semiconductor integrated circuit device for wireless communications, which has an electrostatic breakdown protecting circuit capable of protecting the IC against the positive/negative static electricities.

15 (5) It is possible to provide a semiconductor integrated circuit device for wireless communications, which has a protective circuit capable of protecting a low-frequency circuit (including a circuit of an intermediate-frequency band) and a circuit of a high-
20 frequency band against the electrostatic breakdown.

(6) It is possible to provide a semiconductor integrated circuit device for wireless communications, which is so excellent against the electrostatic breakdown that it does not deteriorate the linearity
25 and gain of the high-frequency circuit.